

DS21Q55DK Quad T1/E1/J1 Transceiver Design Kit Daughter Card

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GENERAL DESCRIPTION

The DS21Q55DK is an easy-to-use evaluation board for the DS21Q55 quad T1/E1/J1 transceiver. The DS21Q55DK is intended to be used as a daughter card with the DK101 motherboard or the DK2000 motherboard. The DS21Q55DK comes complete with a DS21Q55 quad SCT, transformers, termination resistors, configuration switches, line-protection circuitry, network connectors, and motherboard connectors. The DK101/DK2000 motherboard and Dallas' ChipView software give point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status. An on-board FPGA contains mux logic to connect framer ports to one another or to the DK2000 in a variety of configurations.

Each DS21Q55DK is shipped with a free DK101 motherboard. For complex applications, the DK2000 high-performance demo kit motherboard can be purchased separately.

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ORDERING INFORMATION

PART	DESCRIPTION
DS21Q55DK	DS21Q55 Demo Kit Daughter Card (with included DK101 Motherboard)

FEATURES

- Demonstrates Key Functions of DS21Q55 Quad T1/E1/J1 Transceiver
- Includes DS21Q55 Quad LIU, Transformers, BNC, and RJ45 Network Connectors and Termination Passives
- Compatible with DK101 and DK2000 Demo Kit Motherboards
- DK101/DK2000 and ChipView Software Provide Point-and-Click Access to the DS21Q55 Register Set
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- Memory-Mapped FPGA Provides Flexible Clock/Data/Sync Connections Among Framer Ports and DK2000 Motherboard
- LEDs for Loss-of-Signal and Interrupt Status
- Easy-to-Read Silk-Screen Labels Identify the Signals Associated with All Connectors, Jumpers and LEDs
- Network Interface Protection for Overvoltage and Overcurrent Events

DESIGN KIT CONTENTS

- DS21Q55DK Design Kit Daughter Card
- DK101 Low-Cost Motherboard
- CD-ROM
 - ChipView Software
 - DS21Q55DK Data Sheet
 - DK101 Data Sheet
 - DS21Q55 Data Sheet
 - DS21Q55 Errata Sheet

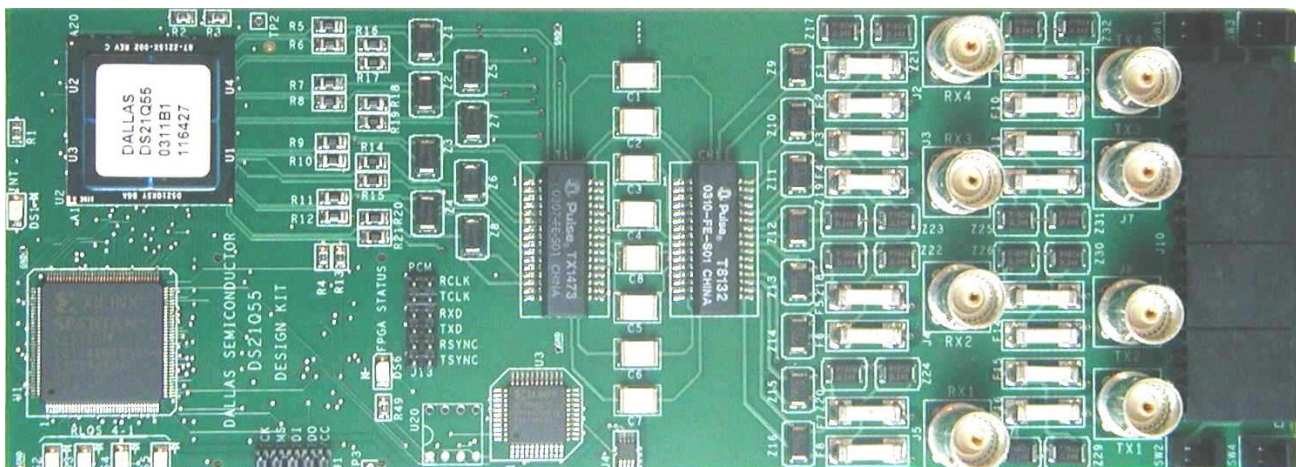


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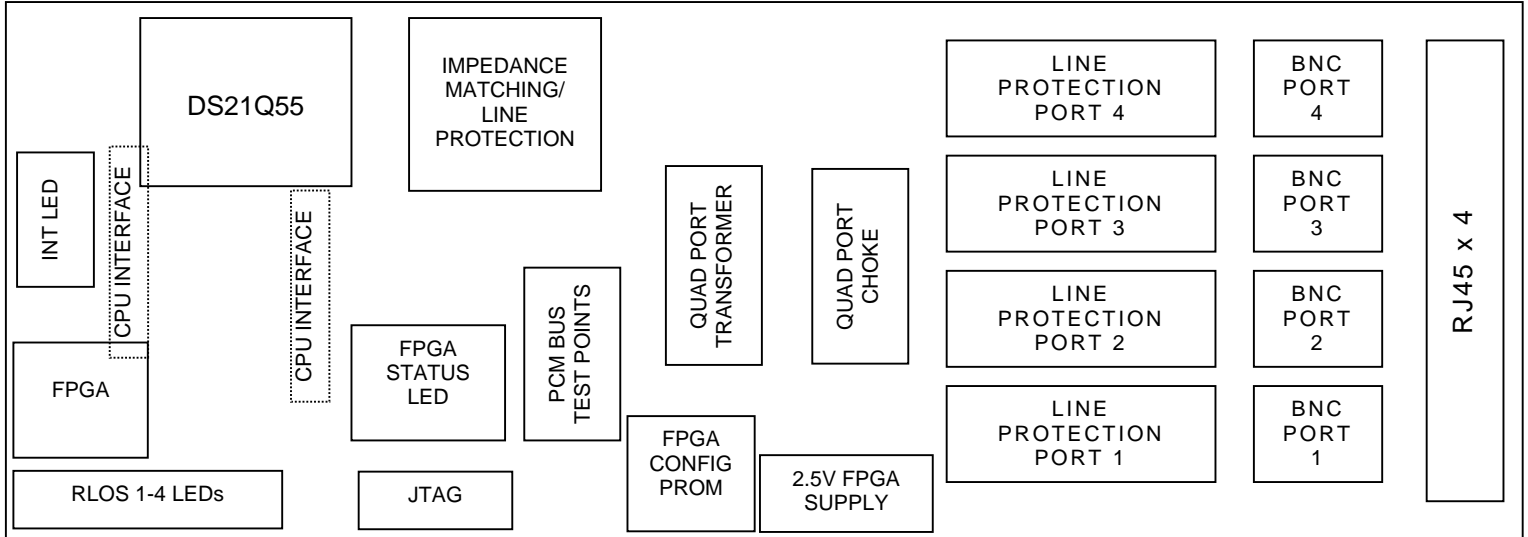
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COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1–C8	8	0.22 μ F, 50V capacitors	Phycomp	PCF1150CT-ND
C9, C10, C12, C18, C22–C33, C35, C38–C43	23	0.1 μ F 10%, 16V ceramic capacitors (0603)	Phycomp	06032R104K7B20D
C11, C13–C15	4	0.1 μ F 10%, 25V ceramic capacitors (1206)	Panasonic	ECJ-3VB1E104K
C16, C17, C19–C21, C34, C36, C45	8	1 μ F 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C37, C44	2	10 μ F 20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
CH1	1	Quad port choke	Pulse	T8132
DS1	1	LED, red, SMD	Panasonic	LN1251C
DS2–DS6	5	LED, green, SMD	Panasonic	LN1351C
F1–F16	16	1.25A, 250V fuse, SMT	Teccor	F1250T
J1	1	10-pin, dual row, vertical jumper	Digi-Key	S2012-05-ND
J2–J9	8	5-pin connectors, BNC right-angle vertical	Cambridge	CP-BNCP-004
J10	1	8-pin 4-port jack, right-angle RJ45	Molex	43223-8140
J11, J12	2	50-pin socket, SMD, dual row, vertical	Samtec	TFM-125-02-S-D-LC
J13	1	12-pin connector, dual row, vertical	Digi-Key	S2012-06-ND
R1, R2, R4	3	10k Ω 1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF1002V
R3, R26, R39, R41, R45	5	10k Ω 5%, 1/10W resistors (0805)	Panasonic	ERJ-6GEYJ103V
R5–R12, R14–R21, R48	17	0 Ω 5%, 1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
R13	1	470 Ω 5%, 1/10W resistor (0805)	Panasonic	ERJ-6GEYJ471V
R22–R25	4	51.1 Ω 1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF51R1V
R27, R28, R38	3	1.0k Ω 1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF1001V
R29–R36	8	61.9 Ω 1%, 1/8W resistors (1206)	Panasonic	ERJ-8ENF61R9V
R37, R47	2	Not populated	Panasonic	Not populated
R40, R42–R44, R46, R49	6	330 Ω 0.1%, 1/10W MF resistors (0805)	Panasonic	ERA-6YEB331V
SW1–SW4	4	6-PIN TH Switch DPDT	Tyco	SSA22
T1	1	XFMR, XMIT/RCV, 1 to 2, SMT 32-pin	Pulse	TX1473
U1	1	XILINX spartan 2.5V FPGA 144-pin, 20 x 20 TQFP	Xilinx	XC2S50-5TQ144C
U2	1	Quad T1/E1/J1 transceiver 256-pin BGA, 0°C to +70°C multichip module	Dallas Semiconductor	DS21Q55
U3	1	1M PROM for FPGA 44-pin TQFP	Xilinx	XC18V01VQ44C_U
U4	1	8-pin μ MAX, SO 2.5V or ADJ	Maxim	MAX1792EUA25
U20	1	Serial configuration EEPROM for XILINX 65kb, 8-DIP	Atmel	AT17LV65EUA-NOPOP
Z1–Z8	8	50A, 6V Sidactor, DO214 SMD	Teccor	P0080SAMC
Z9–Z16	8	500A, 25V Sidactor, DO214 SMD	Teccor	P0300SCMC
Z17–Z32	16	500A, 170V Sidactor, DO214 SMD	Teccor	P1800SCMC

BOARD FLOORPLAN



ERRATA

- Connector J1 has silk-screen mislabeled such that the text TMS and TCK should be swapped. Worded differently, TCK belongs to pin 7 and TMS belongs to pin 9.
- Switches SW1 to SW4 are missing silk screen to indicate which side is grounded. Sliding the switch toward the BNC grounds the BNC shell (E1 mode). For T1 mode the switch should be slid away from the BNC.

BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/telecom. See the DS21Q55DK QuickView data sheet for these files.

Hardware Configuration

Using the DK101 Processor Board:

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V. (The external 5V connector is unused. Additionally, the 'TIM 5V supply' headers are unused.)
- All processor board DIP-switch settings should be in the ON position with exception of the flash-programming switch, which should be OFF.
- From the Programs menu, launch the host application named ChipView.EXE. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

Using the DK2000 Processor Board:

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply may be connected to connector J2.
- From the Programs menu, launch the host application named ChipView.EXE. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

General

- Upon power-up, the RLOS LEDs (green) will not be lit, the INT LED (red) will not be lit, but the FPGA status LED (green) will be lit.
- When operating in E1 mode, slide SW1–SW4 such that the BNC shell is grounded (to the left, as shown in the board floorplan). When operating in T1 mode, ensure that SW1–SW4 are slid to the right as shown in the board floorplan.

Miscellaneous

- Clock frequencies and certain pin bias levels are provided by a register-mapped FPGA, which is on the DS21Q55 daughter card.
- The definition file for this FPGA is named DS21Q55DC_FPGA.def. The definitions are located on page 7. A drop-down menu on the top of the screen allows for switching between definition files.
- All files referenced above are available for download as described in the section marked “BASIC OPERATION”

Quick Setup (Demo Mode)

- The PC will load ChipView offering a choice between DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select Demo Mode.
- The program will request a configuration file, select among the displayed files (DS2155_E1_DSNCOM_DRV.R.cfg or DS2155_T1_DSNCOM_DRV.R.cfg).
- The Demo Mode screen will appear. Upon external loopback, the LOS and OOF indicators will extinguish.
- Note: Demo Mode interacts with the device driver, which is resident in the DK101/DK2000 firmware. The current implementation of this driver is for one device. As such, the demo mode will only interact with **Port 1**. With minor changes, the device driver is extendible to *N* devices.

Quick Setup (Register View)

- The PC will load ChipView offering a choice between DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select Register View.
- The program will request a definition file. Select DS21Q55DC_FPGA.def; through the ‘links’ section this will also load DS21Q55DC.def.
- The Register View Screen will appear, showing the register names, acronyms, and values for the DS21Q55
- Predefined register settings for several functions are available as initialization files.
 - INI files are loaded by selecting the menu File→Reg Ini File→Load Ini File
 - Load the INI file DS21Q55_T1_BERT_ESF.ini
 - After loading the INI file, the following may be observed:
 - The RLOS LEDs (green) light upon external loopback.
 - All four ports of the DS2Q155 begin transmitting a Daly pattern. When external loopback is applied, the BERT bit count registers BBC1–3 and BEC1–3 may be updated by clearing and setting BC1.LC and clicking the ‘Read All’ button.

ADDRESS MAP

DK101 Daughter Card address space begins at 0x81000000.

DK2000 Daughter Card address space begins at:

0x30000000 for slot 0

0x40000000 for slot 1

0x50000000 for slot 2

0x60000000 for slot 3

All offsets given below are relative to the beginning of the daughter card address space (shown above).

Table 1. Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0015	FPGA	Board identification and clock/signal routing
0X1000 to 0X10ff	T1/E1/J1 Transceiver #1	DS21Q55 T1/E1/J1 transceiver, port 1
0X2000 to 0X20ff	T1/E1/J1 Transceiver #2	DS21Q55 T1/E1/J1 transceiver, port 2
0X3000 to 0X30ff	T1/E1/J1 Transceiver #3	DS21Q55 T1/E1/J1 transceiver, port 3
0X4000 to 0X40ff	T1/E1/J1 Transceiver #4	DS21Q55 T1/E1/J1 transceiver, port 4

Registers in the FPGA may be easily modified using the ChipView host-based user-interface software along with the definition file named "DS21Q55DC_FPGA.def."

FPGA Register Map

Table 2. FPGA Register Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0011	MCSR	Control	DS21Q55 MCLK Pin Source
0X0012	TCSR	Control	DS21Q55 TCLK Pin Source
0X0013	SYSCCLKT	Control	DS21Q55 TSYSCCLK Pin Setting
0X0014	SYSCCLKR	Control	DS21Q55 RSYSCCLK Pin Setting
0X0015	SYNC1	Control	DS21Q55 TSYNC Source
0X0016	SYNC2	Control	DS21Q55 TSSYNC Source
0X0017	SYNC3	Control	DS21Q55 RSYNC Source
0X0018	TSERS	Control	TSER Source
0X0019	PRSER	Control	PCM RSER Source
0X001A	PSYNC	Control	PCM RSYNC/TSYNC Source
0X001B	PCLK	Control	PCM RCLK/TCLK Source

ID REGISTERS

BID: BOARD ID (Offset=0X0000)

BID is read only with a value of 0xD

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset=0X0002)

XBIDH is read only with a value of 0x0

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset=0X0003)

XBIDM is read only with a value of 0x1

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset=0X0004)

XBIDL is read only with a value of 0x6

BREV: BOARD FAB REVISION (Offset=0X0005)

BREV is read only and displays the current fab revision

AREV: BOARD ASSEMBLY REVISION (Offset=0X0006)

AREV is read only and displays the current assembly revision

PREV: PLD REVISION (Offset=0X0007)

PREV is read only and displays the current PLD firmware revision

CONTROL REGISTERS

Register Name: **MCSR**

Register Description: **DS21Q55 MCLK Pin Source**

Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	MSRCB	MSRCA
Default	—	—	—	—	—	—	1	1

Bit 0: DS21Q55 Port 1 and 3 MCLK Source (MSRCA)

0 = Connect MCLK 1 (controls port 1 and 3) to the 1.544MHz clock

1 = Connect MCLK 1 (controls port 1 and 3) to the 2.048MHz clock

Bit 1: DS21Q55 Port 2 and 4 MCLK Source (MSRCA)

0 = Connect MCLK 2 (controls port 2 and 4) to the 1.544MHz clock

1 = Connect MCLK 2 (controls port 2 and 4) to the 2.048MHz clock

Register Name: **TCSR**

Register Description: **DS21Q55 TCLK Pin Source**

Register Offset: **0x0012**

Bit #	7	6	5	4	3	2	1	0
Name	T4S1	T4S0	T3S1	T3S0	T2S1	T2S0	T1S1	T1S0
Default	0	0	0	0	0	0	0	0

Bit 0 to 1: DS21Q55 Port 1 TCLK Source (T1S0, T1S1)

The source for TCLK 1 is Defined as shown in Table 3.

Bit 2 to 3: DS21Q55 Port 2 TCLK Source (T2S0, T2S1)

The source for TCLK 2 is Defined as shown in Table 3.

Bit 4 to 5: DS21Q55 Port 3 TCLK Source (T3S0, T3S1)

The source for TCLK 3 is Defined as shown in Table 3.

Bit 6 to 7: DS21Q55 Port 4 TCLK Source (T4S0, T4S1)

The source for TCLK 3 is Defined as shown in Table 3.

Table 3. TCLKx Source Definition

TxS1, TxS0	TCLK CONNECTION
00	Drive TCLK _x with the 1.544MHz clock
01	Drive TCLK _x with the 2.048MHz clock
10	Drive TCLK _x with RCLK _x
11	N/A

Register Name: **SYCLKT**Register Description: **DS21Q55 TSYCLK Pin Setting**Register Offset: **0x0013**

Bit #	7	6	5	4	3	2	1	0
Name	R4S1	R4S0	R3S1	R3S0	R2S1	R2S0	R1S1	R1S0
Default	0	0	0	0	0	0	0	0

Bit 0 to 1: DS21Q55 Port 1 TSYCLK Source (R1S0, R1S1)

The source for TSYCLK 1 is Defined as shown in Table 4.

Bit 2 to 3: DS21Q55 Port 2 TSYCLK Source (R2S0, R2S1)

The source for TSYCLK 2 is Defined as shown in Table 4.

Bit 4 to 5: DS21Q55 Port 3 TSYCLK Source (R3S0, R3S1)

The source for TSYCLK 3 is Defined as shown in Table 4.

Bit 6 to 7: DS21Q55 Port 4 TSYCLK Source (R4S0, R4S1)

The source for TSYCLK 4 is Defined as shown in Table 4.

Table 4. TSYCLK_x Source Definition

RxS1, RxS0	TSYCLK _x CONNECTION
00	Drive TSYCLK _x with the 1.544MHz clock
01	Drive TSYCLK _x with the 2.048MHz clock
10	Drive TSYCLK _x with 8.192MHz clock
11	Drive TSYCLK _x with DS21Q55 Port _x BPCLK

Register Name: **SYCLKR**Register Description: **DS21Q55 RSYCLK Pin Setting**Register Offset: **0x0014**

Bit #	7	6	5	4	3	2	1	0
Name	T4S1	T4S0	T3S1	T3S0	T2S1	T2S0	T1S1	T1S0
Default	0	0	0	0	0	0	0	0

Bit 0 to 1: DS21Q55 Port 1 RSYCLK Source (T1S0, T1S1)

The source for RSYCLK 1 is Defined as shown in Table 5.

Bit 2 to 3: DS21Q55 Port 2 RSYCLK Source (T2S0, T2S1)

The source for RSYCLK 2 is Defined as shown in Table 5.

Bit 4 to 5: DS21Q55 Port 3 RSYCLK Source (T3S0, T3S1)

The source for RSYCLK 3 is Defined as shown in Table 5.

Bit 6 to 7: DS21Q55 Port 4 RSYCLK Source (T4S0, T4S1)

The source for RSYCLK 4 is Defined as shown in Table 5.

Table 5. RSYCLK_x Source Definition

TxS1, TxS0	RSYCLK _x CONNECTION
00	Drive RSYCLK _x with the 1.544MHz clock
01	Drive RSYCLK _x with the 2.048MHz clock
10	Drive RSYCLK _x with 8.192MHz clock
11	Drive RSYCLK _x with DS21Q55 Port _x BPCLK

Register Name: **SYNC1**Register Description: **DS21Q55 TSYNC Pin Source**Register Offset: **0x0015**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	T4SRC	T3SRC	T2SRC	T1SRC
Default	—	—	—	—	0	0	0	0

Bit 0: DS21Q55 Port 1 TSYNC Source (T1SRC)

0 = TSYNC 1 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 1 with RSYNC 1

Bit 1: DS21Q55 Port 2 TSYNC Source (T2SRC)

0 = TSYNC 2 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 2 with RSYNC 2

Bit 2: DS21Q55 Port 3 TSYNC Source (T3SRC)

0 = TSYNC 3 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 3 with RSYNC 3

Bit 3: DS21Q55 Port 4 TSYNC Source (T4SRC)

0 = TSYNC 4 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSYNC 4 with RSYNC 4

Note: When driving TSYNCx with RSYNCx the corresponding DS21Q55 port should be configured such that TSYNCx is an input (IOCR1.1 = 0) and RSYNCx is an output (IOCR1.4 = 0).

Register Name: **SYNC2**Register Description: **DS21Q55 TSSYNC Pin Source**Register Offset: **0x0016**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	T4SRC	T3SRC	T2SRC	T1SRC
Default	—	—	—	—	0	0	0	0

Bit 0: DS21Q55 Port 1 TSSYNC Source (T1SRC)

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 1 with RSYNC 1

Bit 1: DS21Q55 Port 2 TSSYNC Source (T2SRC)

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 2 with RSYNC 2

Bit 2: DS21Q55 Port 3 TSSYNC Source (T3SRC)

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 3 with RSYNC 3

Bit 3: DS21Q55 Port 4 TSSYNC Source (T4Source)

0 = Not using transmit-side elastic store, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive TSSYNC 4 with RSYNC 4

Note: When driving TSSYNCx with RSYNCx the corresponding DS21Q55 port should be configured such that RSYNCx is an output (IOCR1.4 = 0).

Register Name: **SYNC3**

Register Description: **DS21Q55 RSYNC Pin Setting**

Register Offset: **0x0017**

Bit #	7	6	5	4	3	2	1	0
Name	RSOR1	RSOR0	—	—	R4IO	R3IO	R2IO	R1IO
Default	0	0	—	—	0	0	0	0

Bit 0: DS21Q55 Port 1 RSYNC Setting (R1IO)

0 = RSYNC 1 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 1 with RSYNC_x as shown in Table 6

Bit 1: DS21Q55 Port 2 RSYNC Setting (R2IO)

0 = RSYNC 2 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 2 with RSYNC_x as shown in Table 6

Bit 2: DS21Q55 Port 3 RSYNC Setting (R3IO)

0 = RSYNC 3 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 4 with RSYNC_x as shown in Table 6

Bit 3: DS21Q55 Port 4 RSYNC Setting (R4IO)

0 = RSYNC 4 is an output, tri-state corresponding FPGA driver pin (weak pulldown)

1 = Drive RSYNC 4 with RSYNC_x as shown in Table 6

Note: When driving RSYNC_y with RSYNC_x the corresponding DS21Q55 port should be configured such that RSYNC_x is an output (IOCR1.4 = 0) and RSYNC_y is an input (IOCR1.4 = 1).

Table 6. RSYNC_x Function Definition

RSOR1, RSOR0	MASTER RSYNC DESIGNATION
00	RSYNC 1 is used to drive other RSYNC pins (providing R _x IO = 1)
01	RSYNC 2 is used to drive other RSYNC pins (providing R _x IO = 1)
10	RSYNC 3 is used to drive other RSYNC pins (providing R _x IO = 1)
11	RSYNC 4 is used to drive other RSYNC pins (providing R _x IO = 1)

Register Name: **TSERS**Register Description: **DS21Q55 TSER Pin Source**Register Offset: **0x0018**

Bit #	7	6	5	4	3	2	1	0
Name	T4S1	T4S0	T3S1	T3S0	T2S1	T2S0	T1S1	T1S0
Default	0	0	0	0	0	0	0	0

Bit 0 to 1: DS21Q55 Port 1 TSER Source (T1S0, T1S1)

The source for TSER 1 is Defined as shown in Table 7.

Bit 2 to 3: DS21Q55 Port 2 TSER Source (T2S0, T2S1)

The source for TSER 2 is Defined as shown in Table 7.

Bit 4 to 5: DS21Q55 Port 3 TSER Source (T3S0, T3S1)

The source for TSER 3 is Defined as shown in Table 7.

Bit 6 to 7: DS21Q55 Port 4 TSER Source (T4S0, T4S1)

The source for TSER 4 is Defined as shown in Table 7.

Table 7. TSERx Source Definition

TxS1, TxS0	TSER _x CONNECTION
00	Tri-state TSER _x (weak pulldown)
01	Drive TSER _x with RSER _x
10	Drive TSER _x with PCM_TXD bus (DK2000 only)
11	N/A

Register Name: **PRSER**Register Description: **PCM RSER Source**Register Offset: **0x0019**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	R1EN	R1EN	R1EN	R1EN
Default	—	—	—	—	0	0	0	0

Bit 0 to 1: PCM RSER Source (R1EN)

0 = Do not drive DS21Q55 Port 1 RSER onto PCM_RSER

1 = Logically OR DS21Q55 Port 1 RSER with selected other RSER pins and drive onto PCM_RSER

Bit 2 to 3: DS21Q55 Port 2 TSER Source (T2S0, T2S1)

0 = Do not drive DS21Q55 Port 2 RSER onto PCM_RSER

1 = Logically OR DS21Q55 Port 2 RSER with selected other RSER pins and drive onto PCM_RSER

Bit 4 to 5: DS21Q55 Port 3 TSER Source (T3S0, T3S1)

0 = Do not drive DS21Q55 Port 3 RSER onto PCM_RSER

1 = Logically OR DS21Q55 Port 3 RSER with selected other RSER pins and drive onto PCM_RSER

Bit 6 to 7: DS21Q55 Port 4 TSER Source (T4S0, T4S1)

0 = Do not drive DS21Q55 Port 4 RSER onto PCM_RSER

1 = Logically OR DS21Q55 Port 4 RSER with selected other RSER pins and drive onto PCM_RSER

Note: PRSER register is for use with the DK2000 only.

Register Name: **PSYNC**Register Description: **PCM RSYNC/TSYNC Source**Register Offset: **0x001A**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	T2SR	T1SR	—	—	R2SR	R1SR
Default	—	—	0	0	—	—	0	0

Bit 0 to 1: PCM_RSYNC Source

R2SR, R1SR	PCM_RSYNC Source
00	PCM_RSYNC is driven by DS21Q55 port 1 RSYNC.
01	PCM_RSYNC is driven by DS21Q55 port 2 RSYNC.
10	PCM_RSYNC is driven by DS21Q55 port 3 RSYNC.
11	PCM_RSYNC is driven by DS21Q55 port 4 RSYNC.

Bit 4 to 5: PCM_TSYNC Source

T2SR, T1SR	PCM_TSYNC Source
00	PCM_TSYNC is driven by DS21Q55 port 1 TSYNC.
01	PCM_TSYNC is driven by DS21Q55 port 2 TSYNC.
10	PCM_TSYNC is driven by DS21Q55 port 3 TSYNC.
11	PCM_TSYNC is driven by DS21Q55 port 4 TSYNC.

Note: PSYNC register is for use with the DK2000 only.

Register Name: **PCLK**Register Description: **PCM RCLK/TCLK Source**Register Offset: **0x001B**

Bit #	7	6	5	4	3	2	1	0
Name	—	TCM	T2SR	T1SR	—	RCM	R2SR	R1SR
Default	—	0	0	0	—	0	0	0

Bit 0 to 2: PCM_RCLK Source

RCM, R2SR, R1SR	PCM_RCLK Source
000	PCM_RCLK is driven by DS21Q55 port 1 RCLK.
001	PCM_RCLK is driven by DS21Q55 port 2 RCLK.
010	PCM_RCLK is driven by DS21Q55 port 3 RCLK.
011	PCM_RCLK is driven by DS21Q55 port 4 RCLK.
100	PCM_RCLK is driven by DS21Q55 port 1 BPCLK.
101	PCM_RCLK is driven by DS21Q55 port 2 BPCLK.
110	PCM_RCLK is driven by DS21Q55 port 3 BPCLK.
111	PCM_RCLK is driven by DS21Q55 port 4 BPCLK.

Bit 4 to 5: PCM_TCLK Source

TCM, T2SR, T1SR	PCM_TCLK Source
000	PCM_TCLK is driven by source used for DS21Q55 port 1 TCLK.
001	PCM_TCLK is driven by source used for DS21Q55 port 2 TCLK.
010	PCM_TCLK is driven by source used for DS21Q55 port 3 TCLK.
011	PCM_TCLK is driven by source used for DS21Q55 port 4 TCLK.
100	PCM_TCLK is driven by DS21Q55 port 1 BPCLK.
101	PCM_TCLK is driven by DS21Q55 port 2 BPCLK.
110	PCM_TCLK is driven by DS21Q55 port 3 BPCLK.
111	PCM_TCLK is driven by DS21Q55 port 4 BPCLK.

Note: PCLK register is for use with the DK2000 only.

FPGA CONTROL EXAMPLES

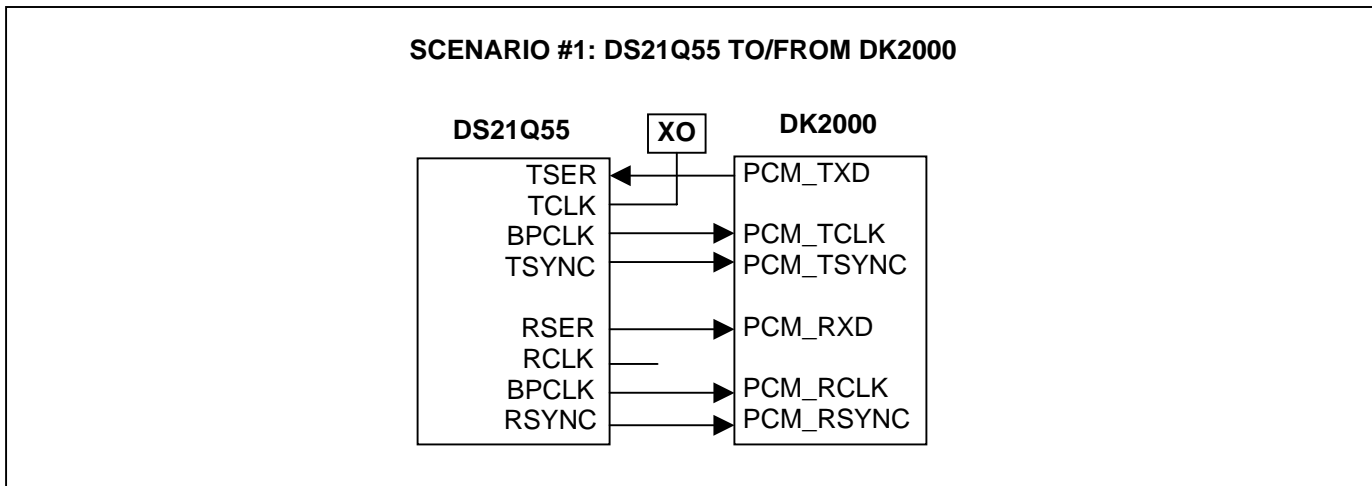


Table 8. FPGA Configuration for Scenario #1 (Port 1, T1 Mode)

REGISTER	SETTING	FUNCTION
MCSR	0X01	Drive DS21Q55 ports 1 and 3 MCLK with 2.048MHz
TCSR	0X00	Drive TCLK with 1.544MHz
SYSCCLKT	0X00	Drive TSYSCCLK with 1.544MHz
SYSCCLKR	0X00	Drive RSYSCCLK with 1.544MHz
SYNC1	0X00	Tri-state FPGA driver pin for DS21Q55 TSYNC1
SYNC2	0X01	Drive TSSYNC1 with RSYNC1
SYNC3	0X00	Tri-state FPGA driver pin for DS21Q55 RSYNC
TSERS	0X02	Drive DS21Q55 TSER1 with data from PCM bus
PRSER	0X01	Drive DS21Q55 RSER1 onto PCM bus
PSYNC	0X00	PCM RSYNC and PCM TSYNC are provided by DS21Q55 port 1 RSYNC and TSYNC (respectively)
PCLK	0X44	PCM RCLK and TCLK are driven by port 1 BPCLK

**SCENARIO #2: EXTERNAL REMOTE LOOPBACK
(FULL BANDWIDTH, NOT JUST PAYLOAD)**

DS21Q55

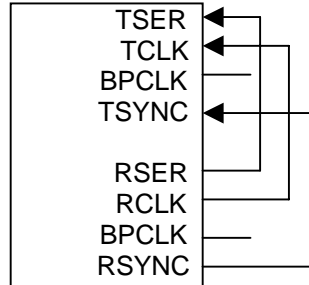


Table 9. FPGA Configuration for Scenario #2 (Port 1, T1 Mode)

REGISTER	SETTING	FUNCTION
MCSR	0X01	Drive DS21Q55 ports 1 and 3 MCLK with 2.048MHz
TCSR	0X02	Drive TCLK1 with RCLK1
SYSCCLKT	0X00	Drive TSYSCCLK with 1.544MHz
SYSCCLKR	0X00	Drive RSYSCCLK with 1.544MHz
SYNC1	0X01	Drive TSYNC1 with RSYNC1
SYNC2	0X01	Drive TSSYNC1 with RSYNC1
SYNC3	0X00	Tri-state FPGA driver pin for DS21Q55 RSYNC
TSERS	0X01	Drive DS21Q55 TSER1 with data from RSER1
PRSER	N/A	Unused
PSYNC	N/A	Unused
PCLK	N/A	Unused

Table 10. DS21Q55 Partial Configuration for Scenario #2 (Port 1, T1 Mode)

REGISTER	SETTING	FUNCTION
IOCR1	TSIO = 0; RSIO = 0	TSYNc is an input, RSYNC is an output
ESCR	TESE = 0; RESE = 0	Bypass Rx and Tx elastic stores
CCR1	TCSS1 = 0; TCSS2 = 0	TCLK is driven by TCLK pin

DS21Q55 INFORMATION

For more information about the DS21Q55, please consult the DS21Q55 data sheet available on our website at www.maxm-ic.com/DS21Q55. Software downloads are also available for this demo kit.

DS21Q55DK INFORMATION

For more information about the DS21Q55DK, including software downloads, please consult the DS21Q55DK data sheet available on our website at www.maxim-ic.com/telecom.

TECHNICAL SUPPORT

For additional technical support, please e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS21Q55DK schematics are featured in the following pages.

DOCUMENT REVISION HISTORY

REVISION DATE	DESCRIPTION
121903	Initial DS21Q55DK data sheet release.
012506	Changed part number for CH1 in <i>Component List</i> from "TX1473" to "T8132."
110106	Updated schematics.

DS21Q55 DESIGN KIT

CONTENTS

1. COVER PAGE
2. DS21Q55 CONTROL AND BACKPLANE
3. PORT 1 AND 2 TX / RX SYSTEM SIDE
4. PORT 3 AND 4 TX / RX SYSTEM SIDE
5. PORT 1 TX / RX ANALOG PATHS
6. PORT 2 TX / RX ANALOG PATHS
7. PORT 3 TX / RX ANALOG PATHS
8. PORT 4 TX / RX ANALOG PATHS
9. TIM ADDRESS DATA BUS CONNECTION
10. FPGA CROSS CONNECT FOR RX / TX SIGNALS
11. FPGA AND CONFIG PROM CONTROL
12. FPGA CLOCK AND DATABUS
13. SUPPLY DECOUPLING
14. SIGNAL CROSS-REFERENCE
15. COMPONENT CROSS-REFERENCE

REVISIONS:

A1: 3/7/2003 - REPLACED THE SYMBOL XC2S50E-U WITH SYMBOL XC2S50-U.

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V3_3

U2

- CS1 P3 CS1*
- CS2 A14 CS2*
- CS3 B5 CS3*
- CS4 K17 CS4*
- WR_RW K3 WR*
- RD_DS N2 RD*
- TP2 JTRST V1B JTRST*
- JTMS W13 JTMS
- JTCLK Y15 JTCLK
- JTDI N1 JTDI
- TP3 JTDI_CON2SCT R4B JTDI
- JTD_SCT2PROM 1 R4B V19 JTD0
- WV_2 WV_2
- A0 U3 A0
- A1 L17 A1
- A2 V2 A2
- A3 T4 A3
- A4 VB A4
- A5 H4 A5
- A6 UB A6
- A7 P4 A7

DS21Q55_U CONTROL

- MCLK1 T1 MCLK1
- MCLK2 W20 MCLK2
- TSTRST U16 TSTRST
- INT* U1 INT*
- BTS P2 BTS
- LIUC K2 LIUC
- MUX U10 MUX
- D0 U11 D_AD0
- D1 J19 D_AD1
- D2 W15 D_AD2
- D3 U7 D_AD3
- D4 U9 D_AD4
- D5 U5 D_AD5
- D6 V4 D_AD6
- D7 U4 D_AD7
- NC1 H1B
- NC2 V17

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- U2 DVDD1<3>
- U5 DVDD1<4>
- B12 DVDD2<1>
- C12 DVDD2<2>
- C16 DVDD2<3>
- D18 DVDD2<4>
- A9 DVDD3<1>
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- B6 DVDD3<3>
- C4 DVDD3<4>
- G20 DVDD4<1>
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- M20 DVDD4<3>
- P18 DVDD4<4>
- P1 DVDD1
- J17 RVD2
- E4 RVD3
- W18 RVD4
- W2 TVDD1
- G19 TVDD2
- D11 TVDD3
- U19 TVDD4

- W4 TVSS1
- GLB TVSS2
- C5 TVSS3
- U1B TVSS4
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- N17 DVSS4<3>
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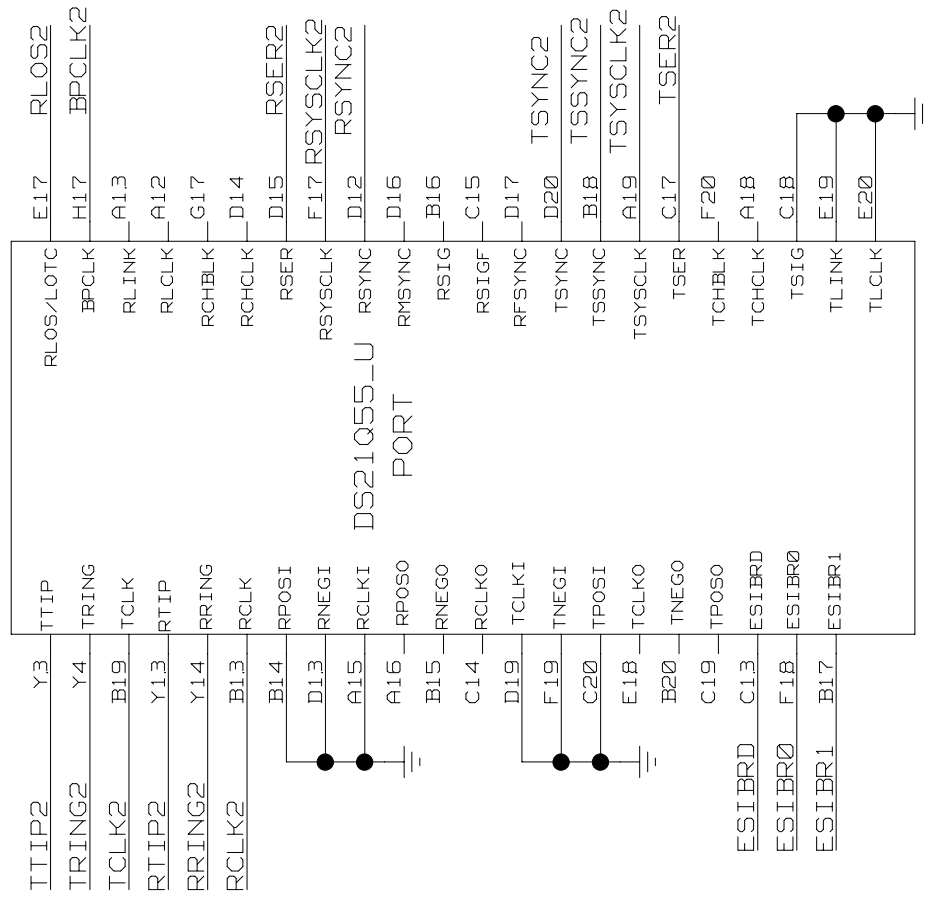
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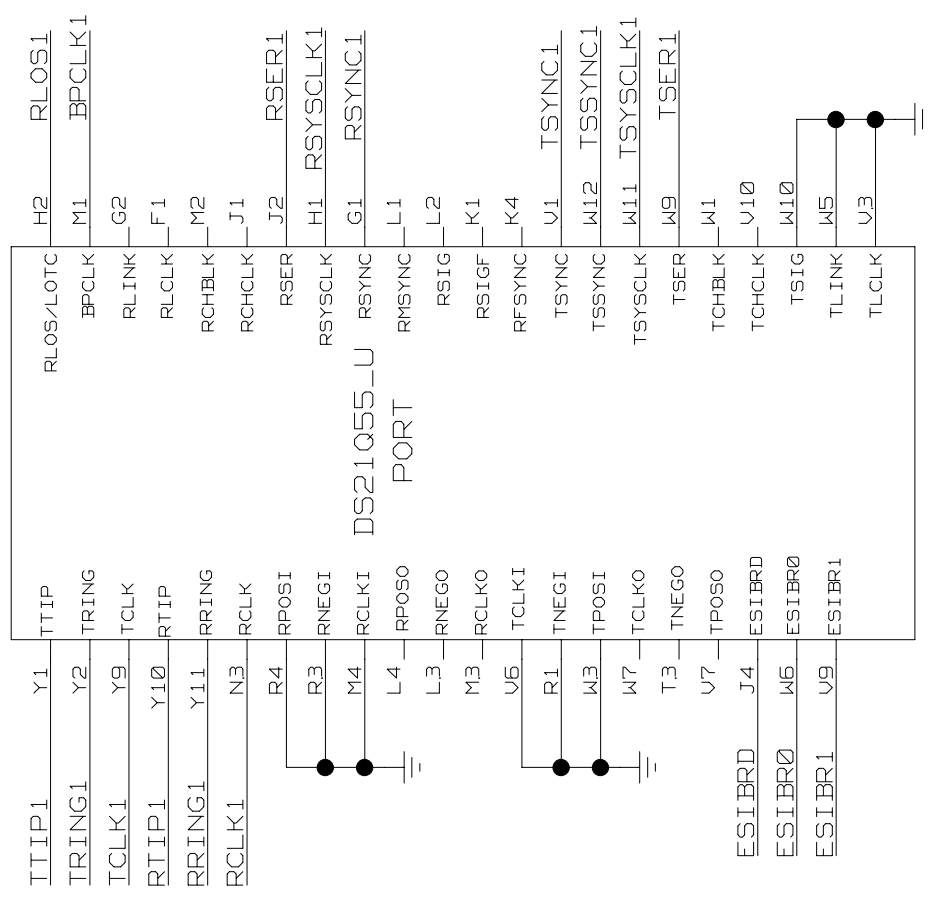
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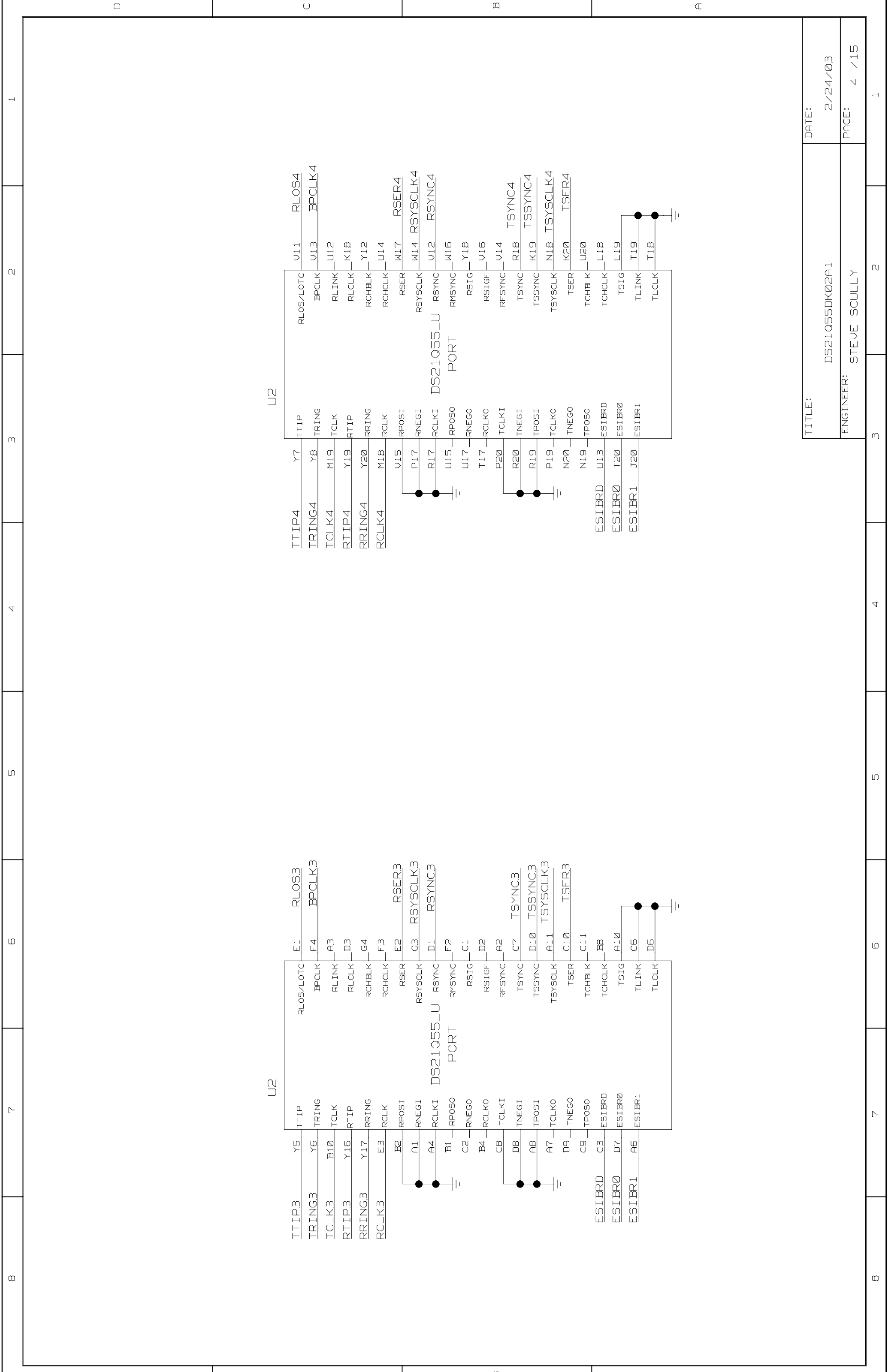
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U2



U2





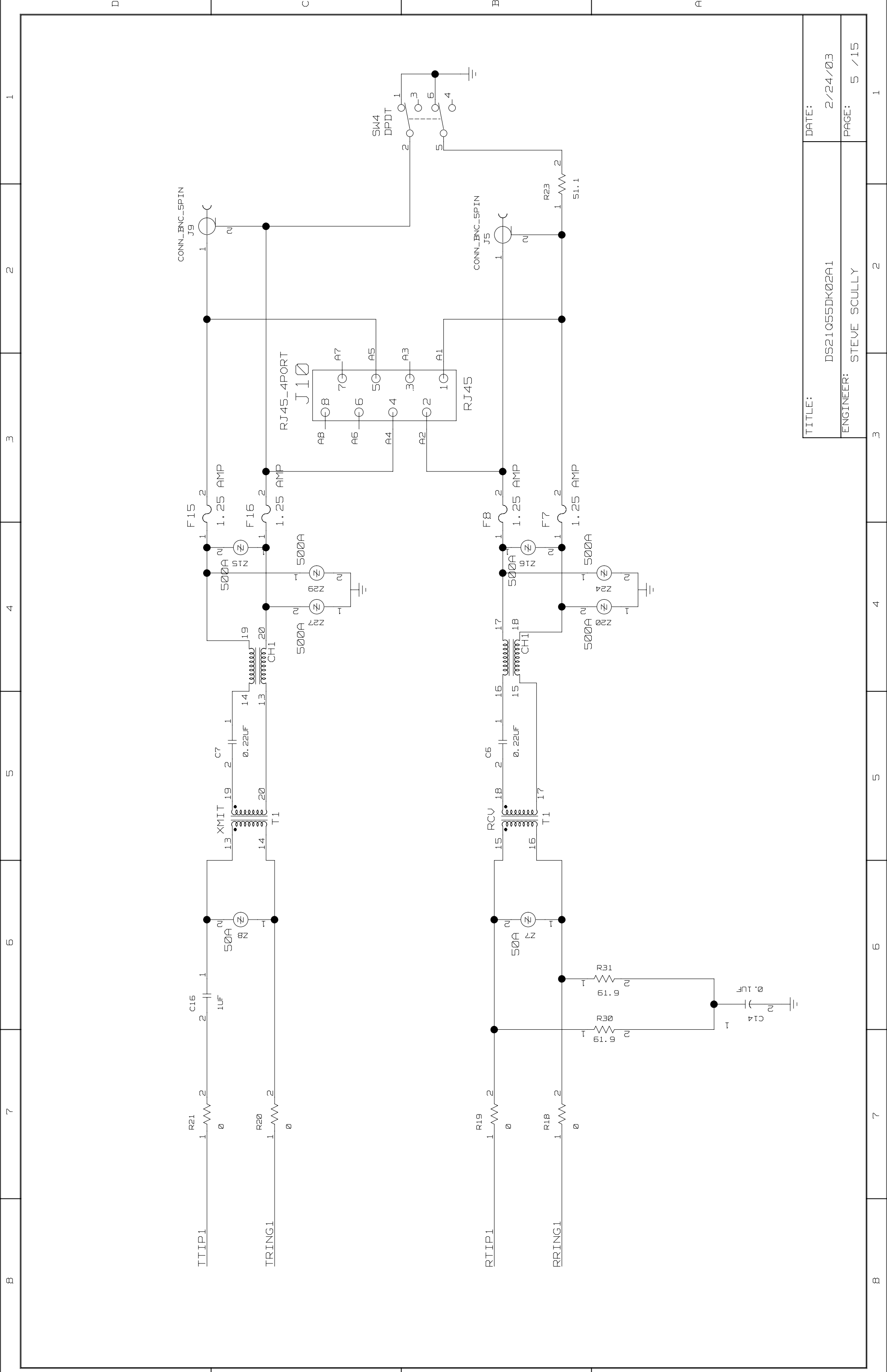
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D C B A

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D C B A



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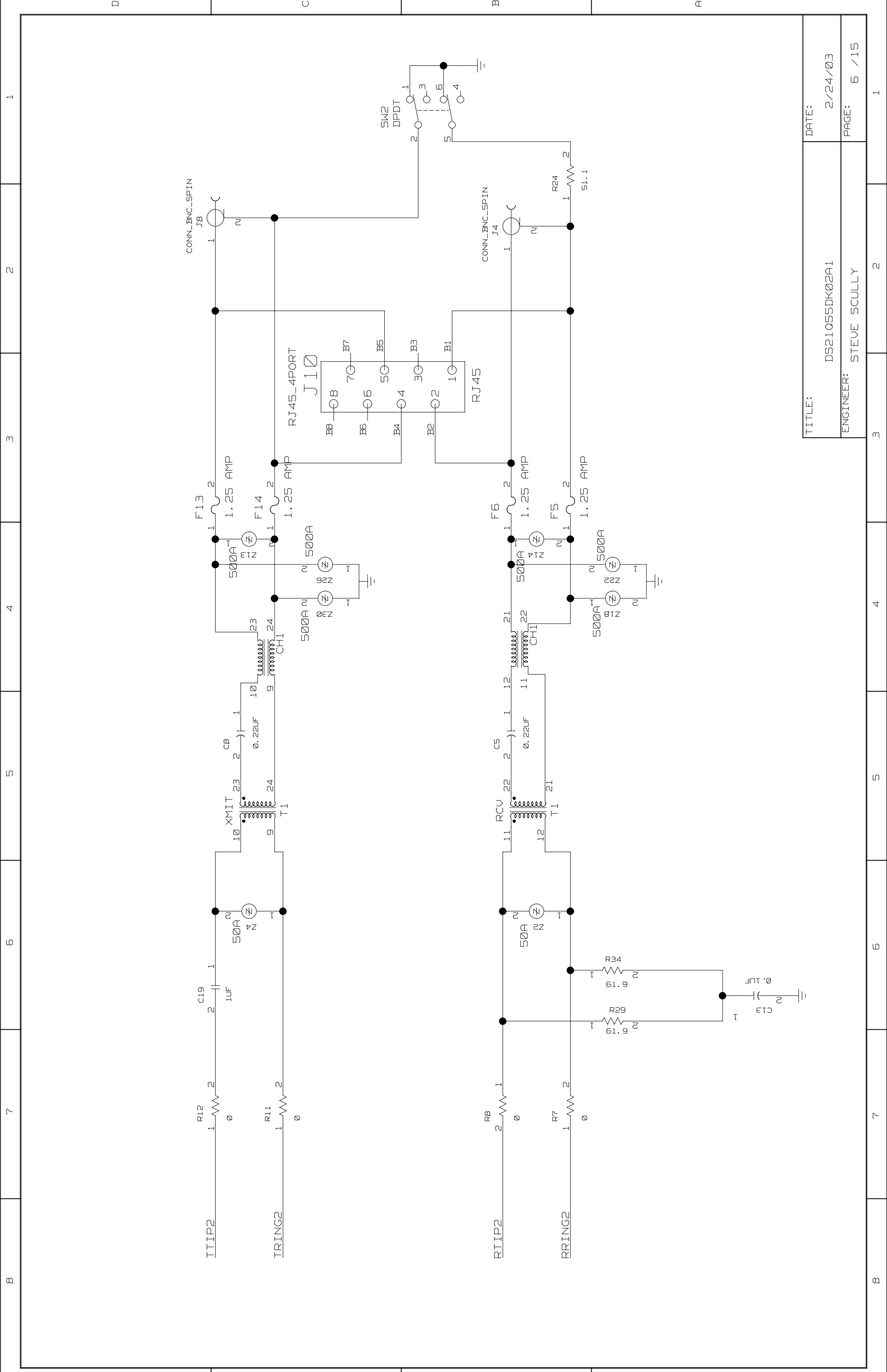
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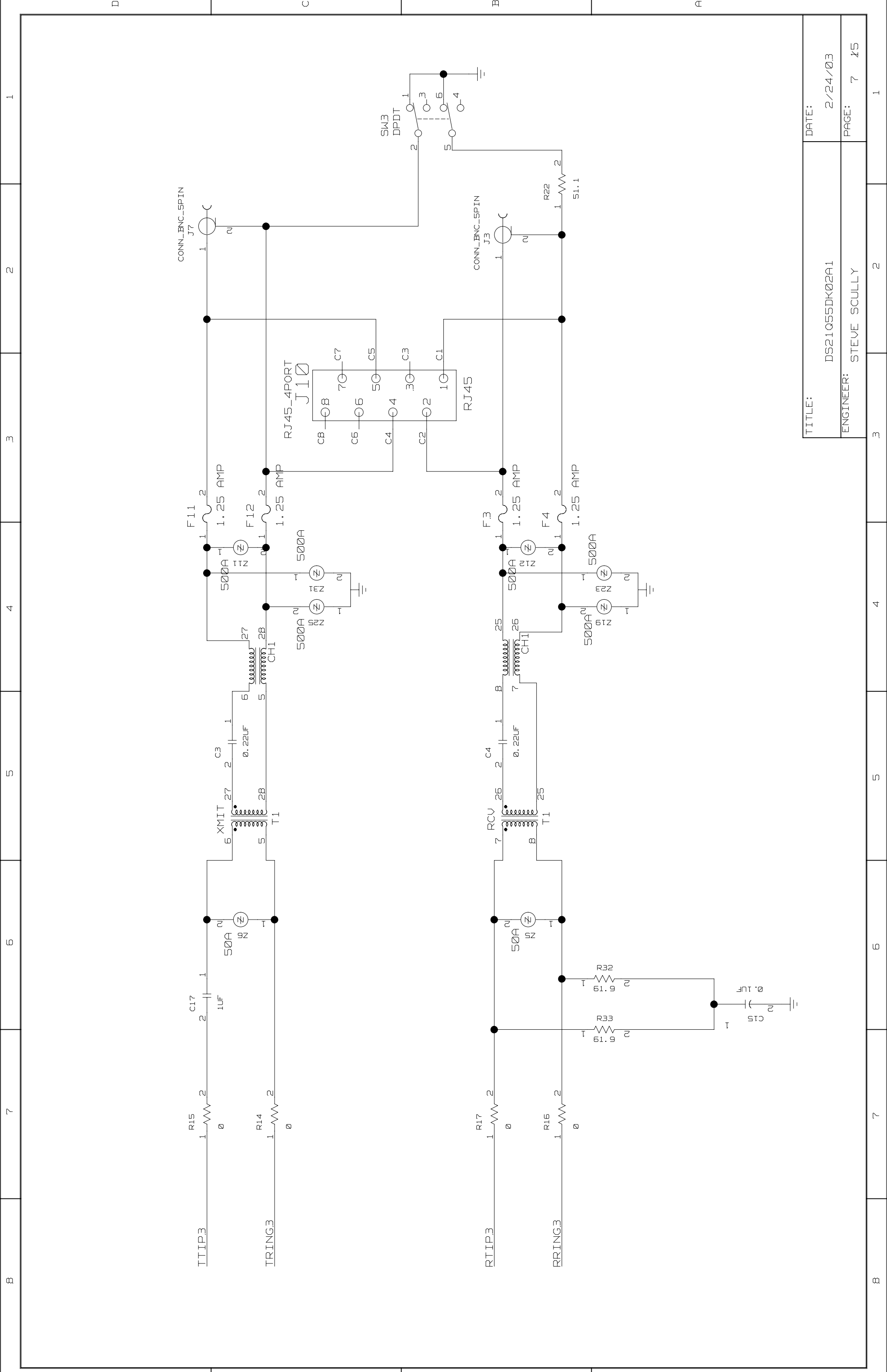
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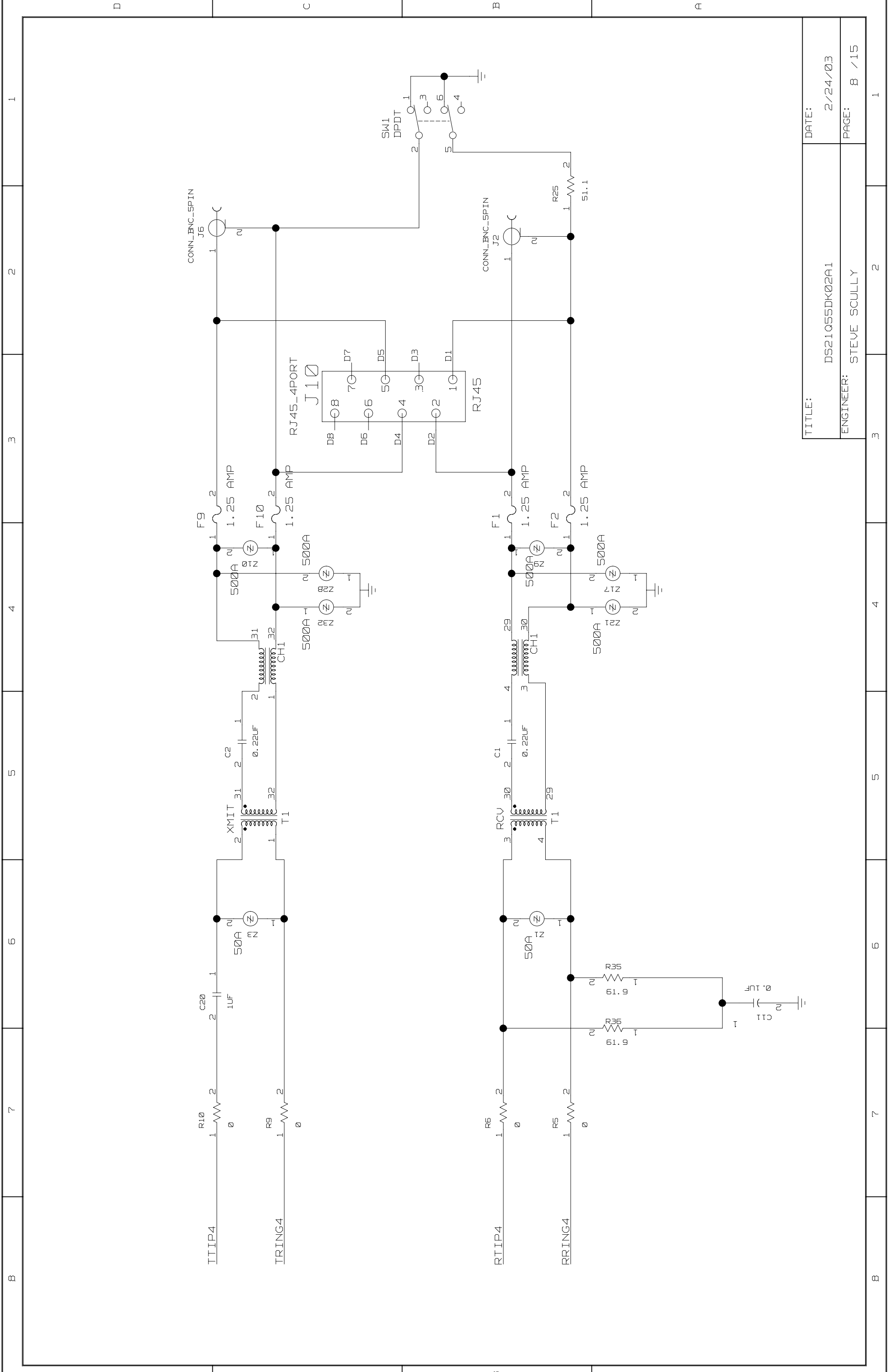
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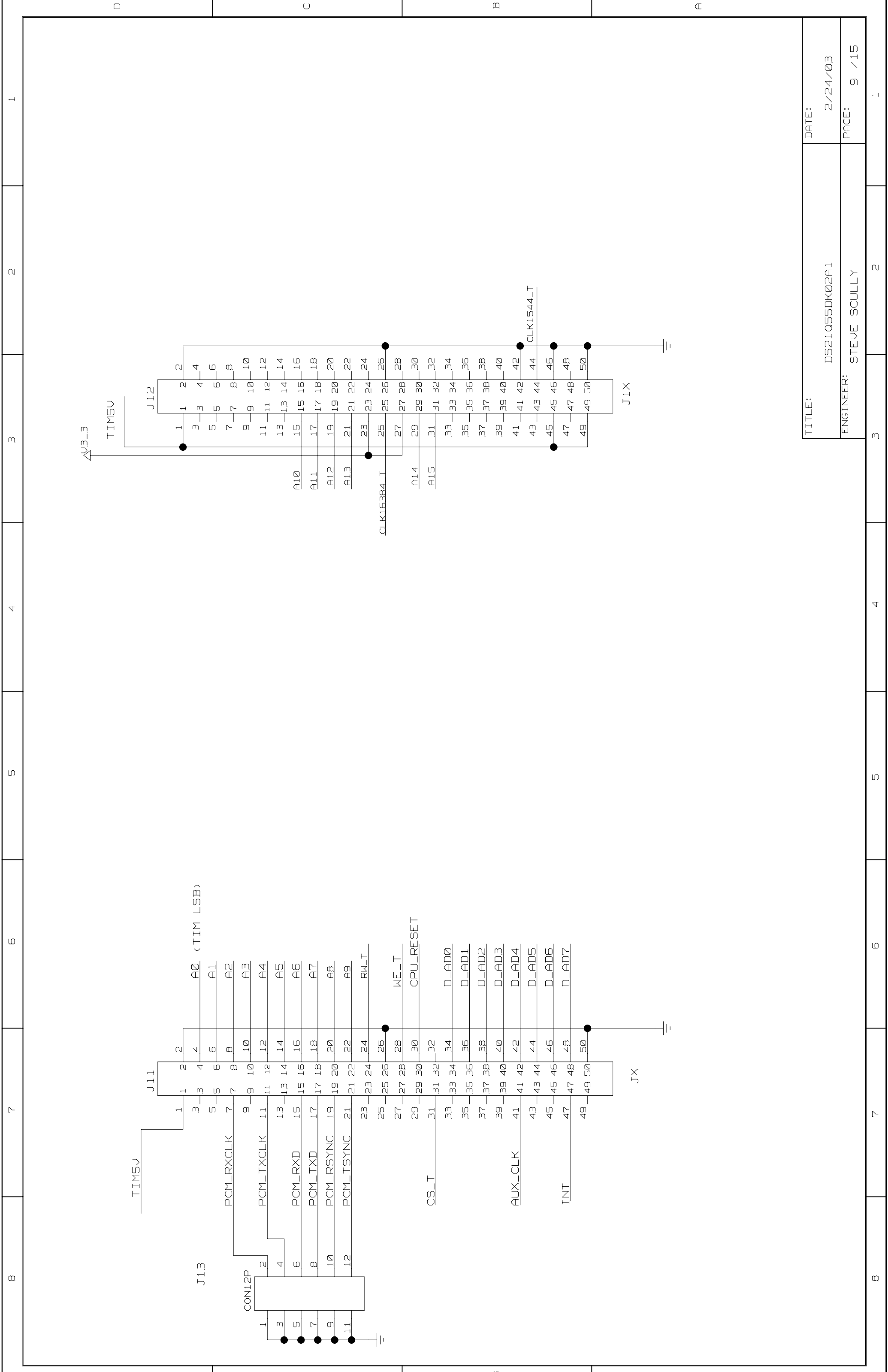


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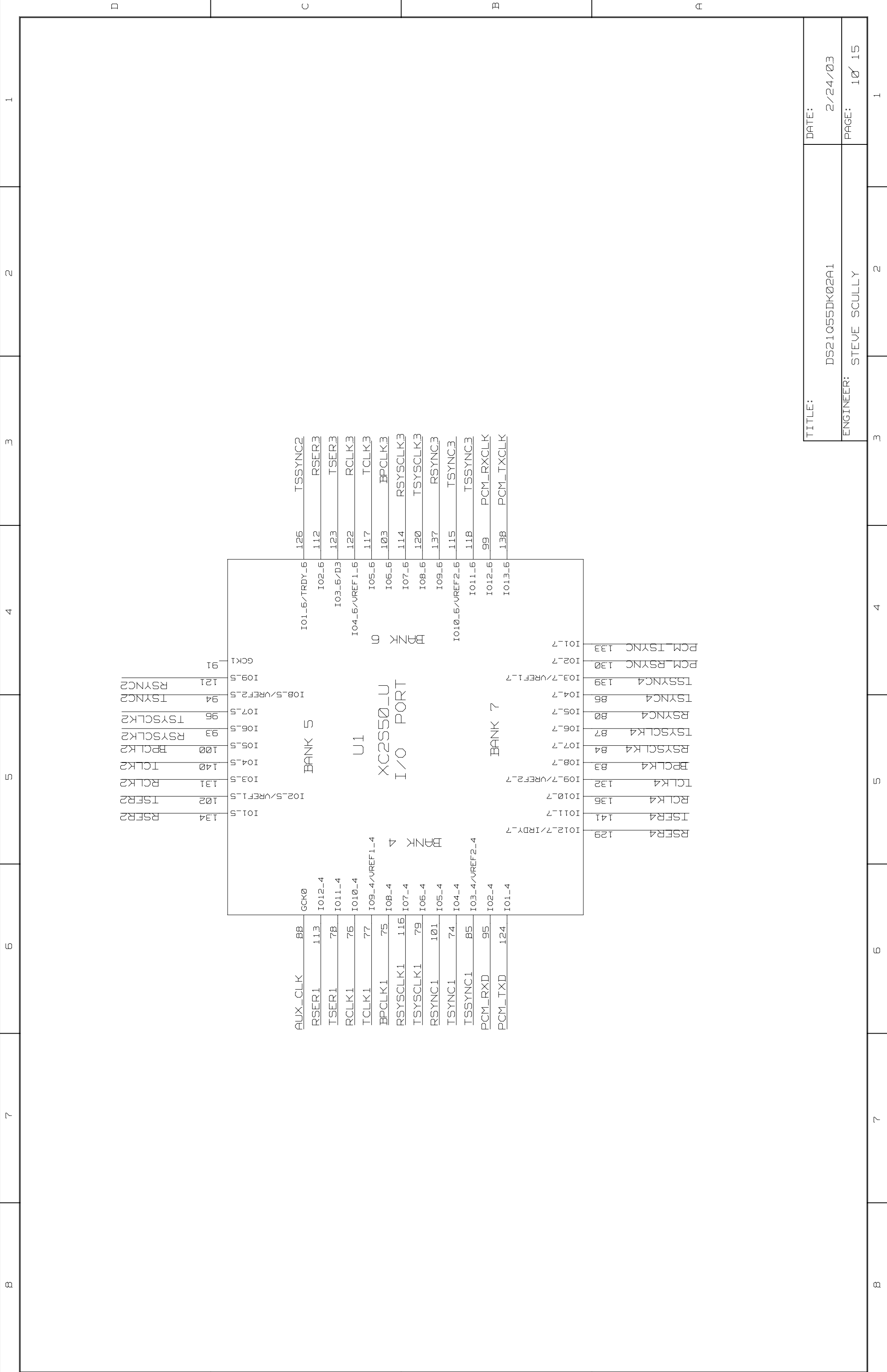


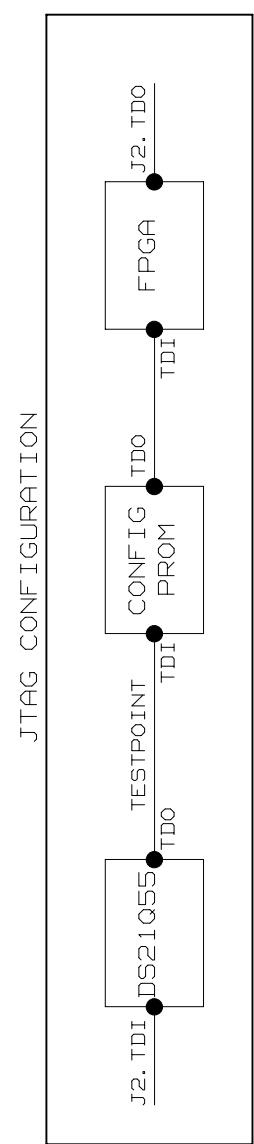
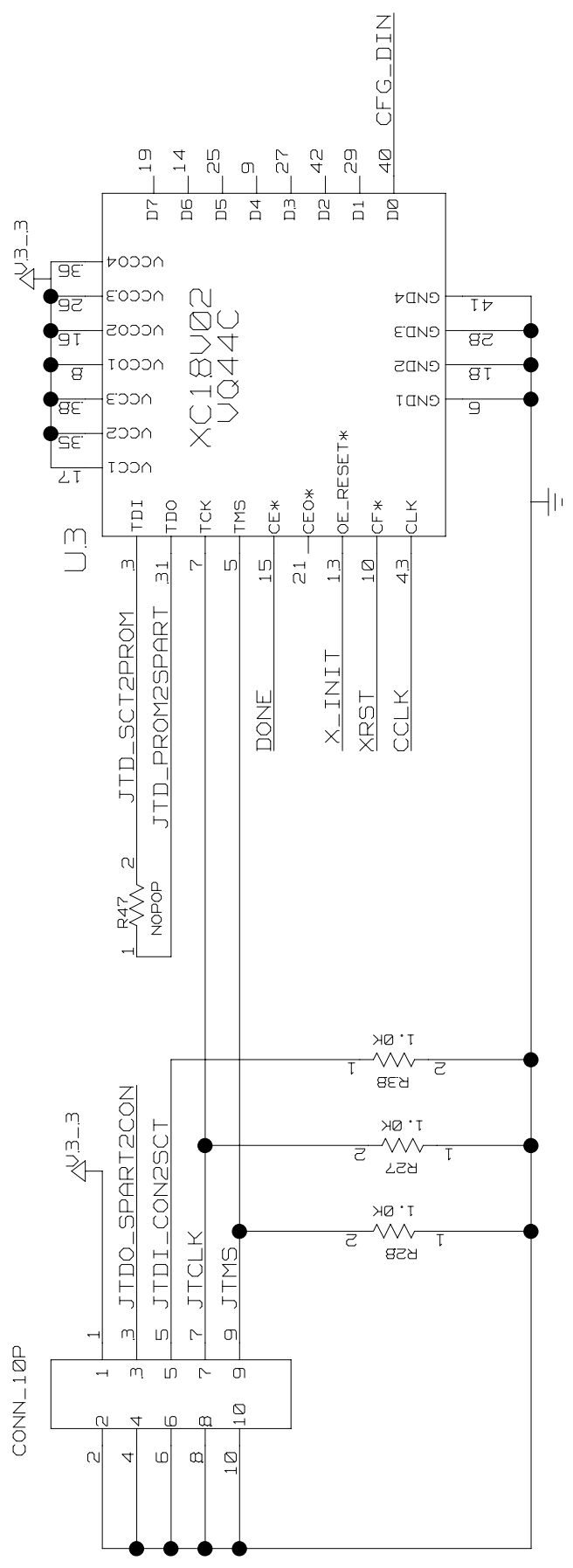
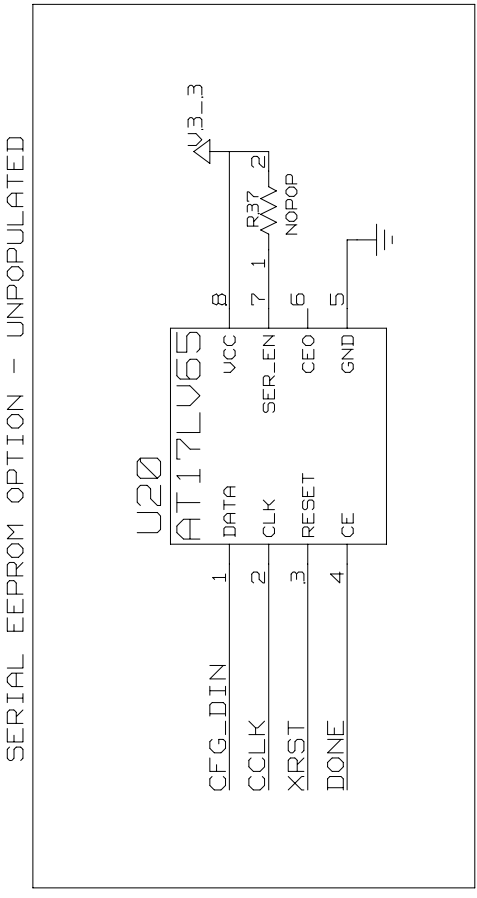
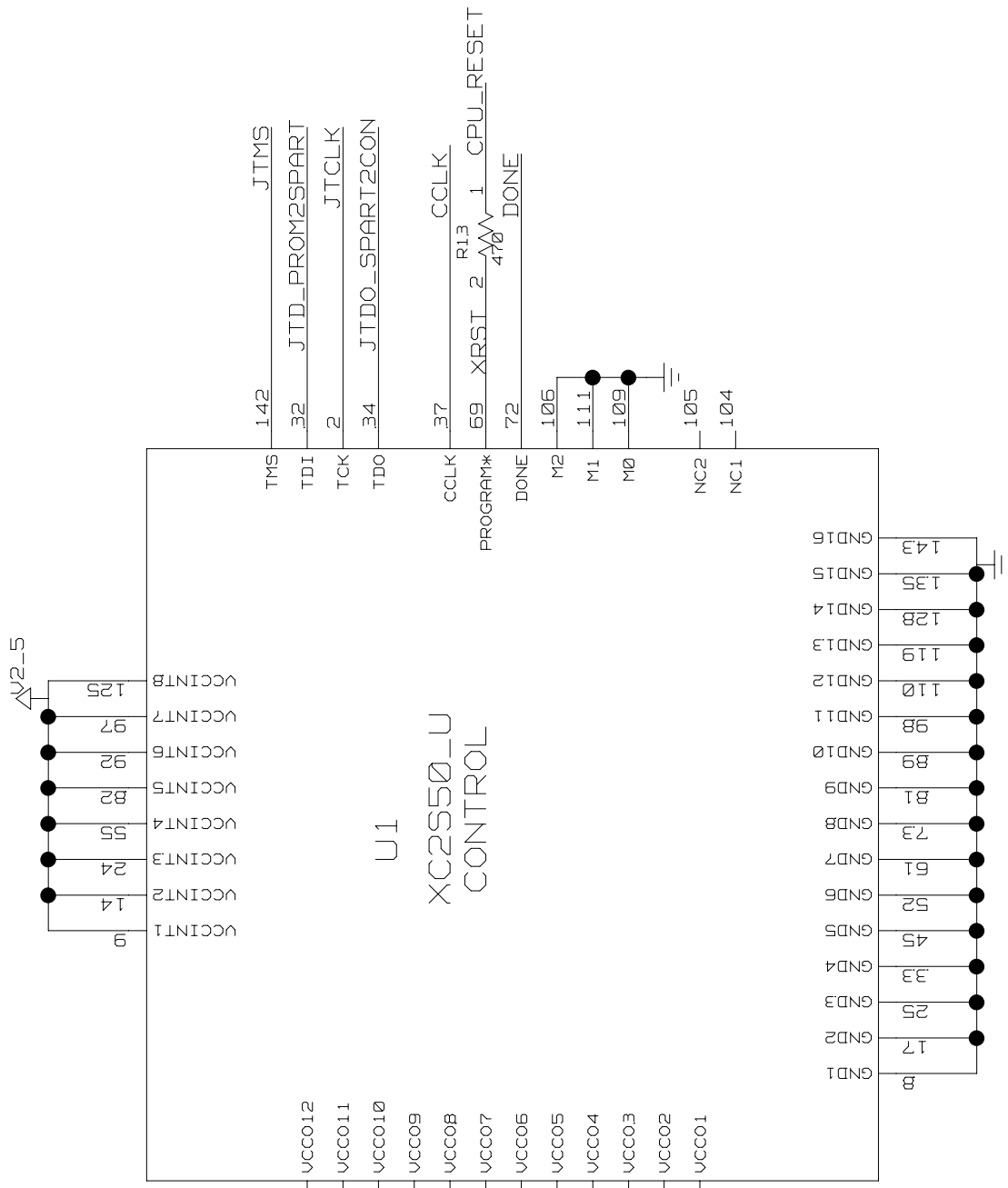
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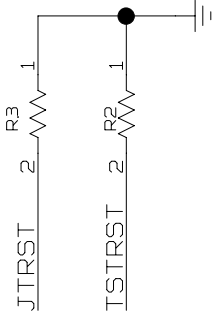
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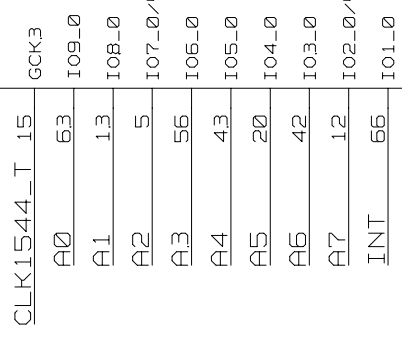
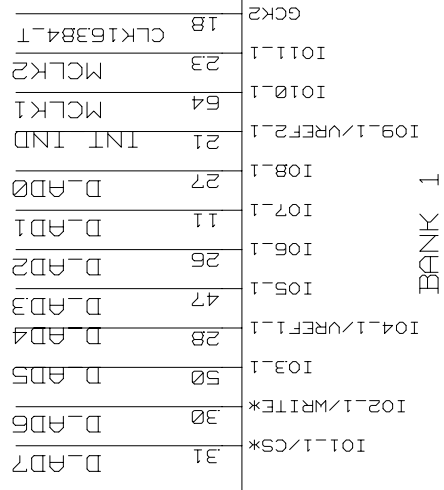
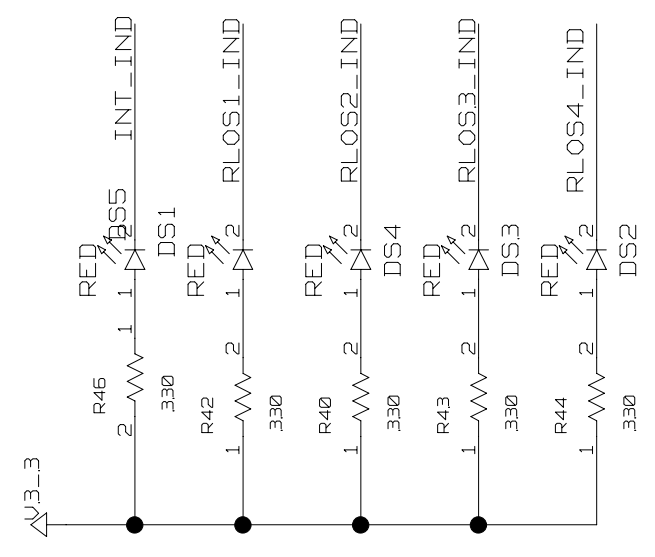
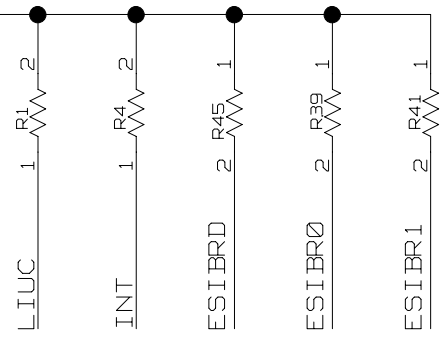




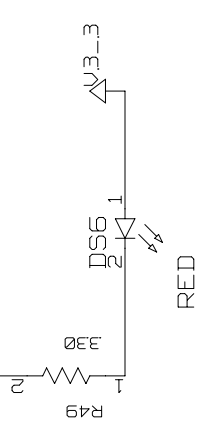
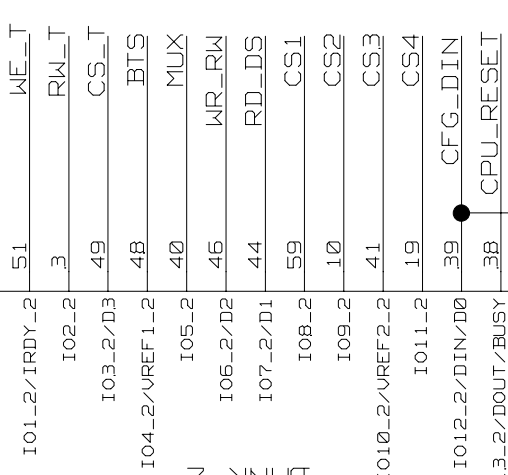
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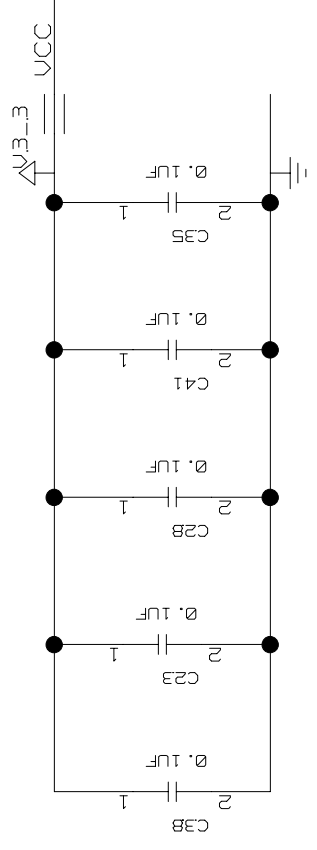
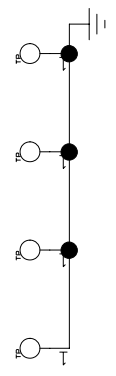
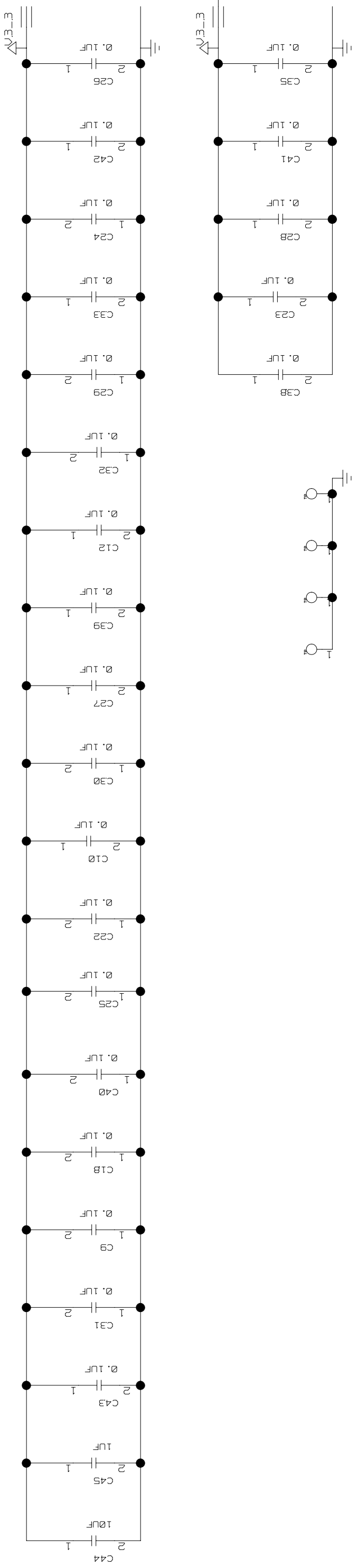
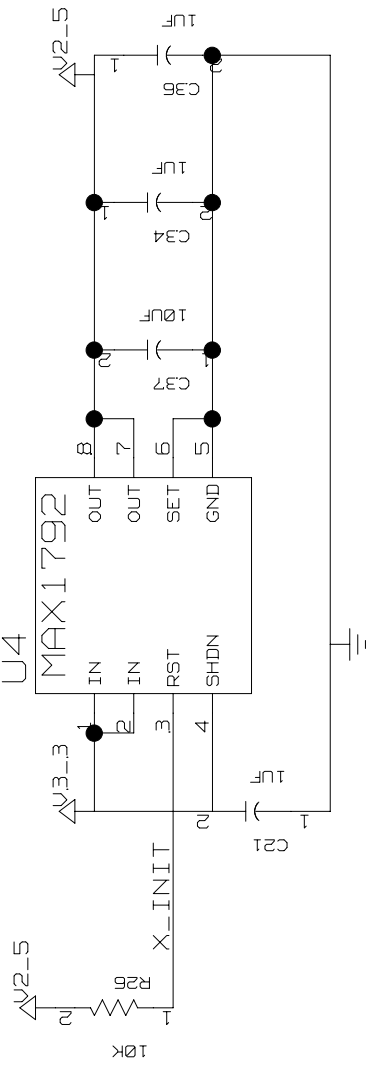
ALL UNMARKED BIAS RESISTORS ARE 10K



U1
XC2S50-U
I/O PORT



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1	2	3	4	5	6	7	8
D	C	B	A	D	C	B	A

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*** Signal Cross-Reference for the entire design ***
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A10     9C3<><
A11     9C3<><
A12     9C3<> 12A4<>
A13     9C3<> 12A4<>
A14     9B3<> 12A4<>
A15     9B3<> 12A3<>
AUX_CLK 9B8<> 10C7<
BPCLK1  3C6<> 10C6<>
BPCLK2  3C1<> 10D5<>
BPCLK3  4C6<> 10C3<>
BPCLK4  4C1<> 10A5<>
BTS     12C1<> 2C3<
CLK     11A6<> 11B8<> 11C1<
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CLK163B4_T 9C4<> 12D3<
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RSYNC3   4B6<> 10B3<>
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TITLE:

ENGINEER:

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<p>*** Part Cross-Reference for the entire design ***</p> <p>C1 CAP 8B5 C2 CAP 8C5 C3 CAP 7C5 C4 CAP 7B5 C5 CAP 6B5 C6 CAP 5B5 C7 CAP 5C5 C8 CAP 6C5 C9 CAP 1.3B7 C10 CAP 1.3B5 C11 CAP 8A6 C12 CAP 1.3B4 C13 CAP 6A6 C14 CAP 5A6 C15 CAP 7A6 C16 CAP 5D6 C17 CAP 7D6 C18 CAP 1.3B7 C19 CAP 6C6 C20 CAP 8C6 C21 CAP 1.3C4 C22 CAP 1.3B5 C23 CAP 1.3B2 C24 CAP 1.3B2 C25 CAP 1.3B6 C26 CAP 1.3B1 C27 CAP 1.3B4 C28 CAP 1.3B2 C29 CAP 1.3B3 C30 CAP 1.3B5 C31 CAP 1.3B7 C32 CAP 1.3B3 C33 CAP 1.3B2 C34 CAP 1.3D3 C35 CAP 1.3B1 C36 CAP 1.3D2 C37 CAP 1.3D3 C38 CAP 1.3B3 C39 CAP 1.3B4 C40 CAP 1.3B6 C41 CAP 1.3B2 C42 CAP 1.3B2 C43 CAP 1.3B8 C44 CAP 1.3B8 C45 CAP 1.3B8 CH1 CHOKE_QUADPORT_T1 5B4 5C4 6B4 6C4 7B4 7C4 8B4 8C4 DS1 LED 1.2B5 DS2 LED 1.2A5 DS3 LED 1.2A5 DS4 LED 1.2A5 DS5 LED 1.2B5 DS6 LED 1.2B2 F1 FUSE 8B4 F2 FUSE 8B4 F3 FUSE 7B4 F4 FUSE 7B4 F5 FUSE 6B3 F6 FUSE 6B3 F7 FUSE 5B4 F8 FUSE 5B4 F9 FUSE 8D4 F10 FUSE 8C4 F11 FUSE 7D4 F12 FUSE 7C4 F13 FUSE 6D3 F14 FUSE 6C3 F15 FUSE 5D4 F16 FUSE 5C4 J1 CONN_10P 1.1B8 J2 CONN_BNC_SPIN 8B2 J3 CONN_BNC_SPIN 7B2 J4 CONN_BNC_SPIN 6B2 J5 CONN_BNC_SPIN 5B2 J6 CONN_BNC_SPIN 8D2</p>	<p>J7 CONN_BNC_SPIN 7D2 J8 CONN_BNC_SPIN 6D2 J9 CONN_BNC_SPIN 5D2 J10 RJ45_B 5C3 6C3 7C3 8C3 J11 CONN_50P2 9D7 J12 CONN_50P2 9D3 J13 CON12P 9D8 R1 RES1 1.2D6 R2 RES1 1.2D7 R3 RES 1.2D7 R4 RES1 1.2D6 R5 RES 8B7 R6 RES 8B7 R7 RES 6B7 R8 RES 6B7 R9 RES 8C7 R10 RES 8D7 R11 RES 6C7 R12 RES 6D7 R13 RES 1.1C2 R14 RES 7C7 R15 RES 7D7 R16 RES 7B7 R17 RES 7B7 R18 RES 5B7 R19 RES 5B7 R20 RES 5C7 R21 RES 5D7 R22 RES 7B2 R23 RES 5B2 R24 RES 6B2 R25 RES 8B2 R26 RES 1.3D4 R27 RES 1.1A7 R28 RES1 1.1A8 R29 RES1 6A6 R30 RES1 5A6 R31 RES1 5A6 R32 RES1 7A6 R33 RES1 7A6 R34 RES1 6A6 R35 RES1 8A6 R36 RES1 8A6 R37 RES1 1.1B7 R38 RES1 1.1A7 R39 RES 1.2C6 R40 RES1 1.2A6 R41 RES 1.2C6 R42 RES1 1.2A6 R43 RES1 1.2A6 R44 RES1 1.2A6 R45 RES 1.2D6 R46 RES1 1.2B6 R47 RES1 1.1A7 R48 RES 2B7 R49 RES1 1.2B2 SW1 SWITCH_DPDT_SLIDE_6P 8C1 SW2 SWITCH_DPDT_SLIDE_6P 6C1 SW3 SWITCH_DPDT_SLIDE_6P 7C1 SW4 SWITCH_DPDT_SLIDE_6P 5C1 T1 XFMR_QUADPORT_T1 5B5 5C5 6B5 6C5 7B5 7C5 8B5 8C5 TP1 TSTPNT_SNG 1.3B3 TP2 TESTPOINT 2B8 TP3 TESTPOINT 2B8 TP24 TSTPNT_SNG 1.3B4 TP25 TSTPNT_SNG 1.3B4 TP26 TSTPNT_SNG 1.3B4 U1 XC2S50_U 10C5 11C3 12C3 U2 DS21055_U 2D7 3C3 3C7 4C3 4C7 U3 XC18V02V044C_U 1.1A6 U4 MAX1792 1.3D4 U20 AT17LV65 1.1C7 Z1 SIDACTOR_2 8B6 Z2 SIDACTOR_2 6B6 Z3 SIDACTOR_2 8C6 Z4 SIDACTOR_2 6C6</p>	<p>Z5 SIDACTOR_2 7B5 Z6 SIDACTOR_2 7C6 Z7 SIDACTOR_2 5B6 Z8 SIDACTOR_2 5C6 Z9 SIDACTOR_2 8B4 Z10 SIDACTOR_2 8C4 Z11 SIDACTOR_2 7C4 Z12 SIDACTOR_2 7B4 Z13 SIDACTOR_2 6C4 Z14 SIDACTOR_2 6B4 Z15 SIDACTOR_2 5C4 Z16 SIDACTOR_2 5B4 Z17 SIDACTOR_2 8A4 Z18 SIDACTOR_2 6A4 Z19 SIDACTOR_2 7A4 Z20 SIDACTOR_2 5A4 Z21 SIDACTOR_2 8A4 Z22 SIDACTOR_2 6A4 Z23 SIDACTOR_2 7A4 Z24 SIDACTOR_2 5A4 Z25 SIDACTOR_2 7C4 Z26 SIDACTOR_2 6C4 Z27 SIDACTOR_2 5C4 Z28 SIDACTOR_2 8C4 Z29 SIDACTOR_2 5C4 Z30 SIDACTOR_2 6C4 Z31 SIDACTOR_2 7C4 Z32 SIDACTOR_2 8C4</p>	<p>D</p>	<p>C</p>	<p>B</p>	<p>A</p>
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